AMENDMENTS TO THE CLAIMS:

1. (Currently amended) A microprocessor, comprising:

a microcode unit for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction.

2. (Original) The microprocessor according to claim 1, wherein each of the embedded logic circuits includes:

a table for performing a table lookup in response to a received instruction; and

a controller responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup for controllably setting each of the control signals required by the microprocessor for executing said received instruction.

3. (Original) The microprocessor of claim 2, wherein the controller includes:

means for setting a control signal to a "1" regardless of its immediately preceding value;

means for setting a control signal to a "0" regardless of its immediately preceding value; and

means for not modifying a control signal from its immediately preceding value.

4. (Original) The microprocessor of claim 3, wherein the controller further includes:

means for setting a control signal to a data state.

5. (Canceled).

6. (Previously presented) The microprocessor according to claim 1, further comprising means for determining which of the control signals are not to be modified for each instruction.

7-8. (Canceled).

9. (Currently amended) A microcode unit in a microprocessor, for outputting control signals, for each of a plurality of instructions, required by said microprocessor for executing said instructions, the microcode unit comprising:

an instruction address input for receiving an instruction address;

a control variable input for receiving a control variable corresponding to a current state of the microprocessor;

a control signal input for receiving all the control signals output by the microcode unit for an immediately preceding instruction; and

a plurality of embedded logic circuits each dedicated for evaluating one unique type of instruction received by the microcode unit and for setting the control signals required for executing said received instruction.

10-19. (Canceled).

20. (Original) A method of providing a state machine decoding, comprising:

decoding a current opcode to provide a decode;

setting required functions signals;

setting exclusive functions outside of the current opcode to a previous state; and

latching results of the decode.

21-22. (Canceled).

23. (New) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises a controller for controllably setting each of the control signals required by the microprocessor for executing said received instruction.

24. (New) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises a controller for controllably setting only each of the control signals required by the microprocessor for executing said received instruction.

25. (New) The microprocessor of claim 1, wherein each of the plurality of embedded logic circuits comprises a table that performs a table lookup in response to a received instruction.

26. (New) The microprocessor of claim 25, wherein said controller is responsive to the control variable, the control signals for an immediately preceding instruction, and to the table lookup.

27. (New) The microprocessor of claim 23, wherein the controller includes means for maintaining a control signal at an immediately preceding value of said control signal.

28. (New) The microprocessor of claim 27, wherein the controller further includes:

means for setting a control signal to a "1" regardless of an immediately preceding value of said control signal; and

means for setting a control signal to a "0" regardless of an immediately preceding value of said control signal.

29. (New) The microprocessor of claim 28, wherein the controller further comprises means for setting a control signal to a data state.

30. (New) The microprocessor according to claim 1, further comprising means for determining at least one of said control signals to be maintained for each instruction.